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[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 9929240 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 9929240 (the "9929240 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

An analysis of US Patent No. 9,929,240 is provided below.
Patent Information
• Title: Memory transistor with multiple charge storing layers and a high work function gate electrode
• Assignee: The original assignee was Cypress Semiconductor Corp. As of May 4, 2019, the patent was assigned to Longitude Flash Memory Solutions Ltd.
• Inventors: Igor Polishchuk, Sagy Charel Levy, Krishnaswamy Ramkumar
• Filing Date: October 26, 2016
• Issue Date: March 27, 2018
• Abstract: "An example memory device includes a channel positioned between and electrically connecting a first diffusion region and a second diffusion region, and a tunnel dielectric layer, a multi-layer charge trapping layer, and a…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 9929240 Patent:

Analysis of Prior Art for U.S. Patent No. 9,929,240

A critical aspect of patent analysis involves examining the prior art cited during the patent's prosecution and in any subsequent legal challenges. This analysis determines whether the invention claimed in the patent was already known and therefore not novel. Under U.S. patent law, specifically 35 U.S.C. § 102, a patent claim is invalid if every element of that claim is present in a single prior art reference. This is known as "anticipation." What follows is an assessment of the most relevant prior art references cited for U.S. Patent No. 9,929,240, focusing on their potential to anticipate the independent claims.

Key Concepts in the '240 Patent

The core of the invention in the '240 patent is a specific multi-layer charge-trapping structure within a non-volatile memory transistor. The key features, as detailed in the independent claims, are:

• A multi-layer charge trapping region: This is the heart of the invention.

• Three specific sub-layers:

1. An "oxygen-rich" nitride layer (also referred to as silicon oxynitride).
2. An…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

Analysis of Obviousness for U.S. Patent No. 9,929,240

A person of ordinary skill in the art (POSA) at the time of the invention would have found the claims of U.S. Patent No. 9,929,240 obvious based on a combination of prior art references. The key features of the '240 patent—a multi-layer charge-trapping region with specific oxygen concentrations and an anti-tunneling layer, combined with a high work function gate electrode—are all taught or suggested by the prior art for the predictable purpose of improving memory cell performance, particularly data retention and program/erase efficiency.

Key Elements of the Invention

The independent claims of the '240 patent, particularly Claim 1, describe a memory transistor with a gate stack comprising:

1. A tunnel dielectric layer.
2. A multi-layer charge trapping region which includes:

An oxygen-rich first nitride layer.

An anti-tunneling oxide layer on top of the first nitride layer.

An oxygen-lean second nitride layer on top of the anti-tunneling layer.

3. A blocking dielectric layer.
4. A high work function gate electrode.

The core…

4. Litigation History of the Patent

Public records reflect that the 9929240 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

• IPValue Management, Inc. et al. v. Western Digital Corporation et al. — 8:25-cv-00119 · U.S. District Court for the Central District of California · filed 2025-01-22 · Settled

• SanDisk Corporation v. IPValue Management, Inc. et al. — 5:25-cv-02389 · U.S. District Court for the Northern District of California · filed 2025-03-07 · Settled

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]