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[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 9824035 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 9824035 (the "9824035 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

Analysis of U.S. Patent No. 9,824,035
Date of Analysis: May 13, 2026
This report provides a summary of United States Patent No. 9,824,035, including its bibliographic details and a plain-language explanation of its independent claims.
Bibliographic Information:
• Title: Memory module with timing-controlled data paths in distributed data buffers
• Assignee: Netlist, Inc.
• Inventors: Hyun Lee, Jayesh R. Bhakta
• Filing Date: February 7, 2017
• Issue Date: November 21, 2017
• Abstract: A memory module is operatable in a memory system with a memory controller. The memory module comprises a module control device mounted on the module board to receive command signals from the memory…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 9824035 Patent:

Analysis of Prior Art for U.S. Patent No. 9,824,035
This analysis details the most relevant prior art cited against U.S. Patent No. 9,824,035. The '935 patent, assigned to Netlist, Inc., describes a memory module with intelligent, distributed data buffers that can learn and adjust for signal timing variations. The key innovation lies in the buffer circuits' ability to obtain timing information from one memory operation (e.g., a write) and use it to control the timing of a subsequent, different operation (e.g., a read).
Under 35 U.S.C. § 102, a patent claim is anticipated if a single prior art reference discloses each and every element of the claim. The following cited references are evaluated for their potential to anticipate the independent claims (1 and 15) of the '935 patent.

Key Cited References and Potential Anticipation:
The following patents were cited during the prosecution of the '935 patent and are considered relevant to its claims.
1. U.S. Patent No. 7,370,143 B2: "Memory Module with a Hub Device for Interfacing Memory Devices and a Memory Controller and Method…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

Analysis of Obviousness for U.S. Patent No. 9,824,035
An analysis of U.S. Patent No. 9,824,035 ('035 patent) and the relevant prior art indicates that the independent claims would have been obvious to a Person Having Ordinary Skill in the Art (PHOSITA) at the time of the invention. The primary inventive concept—a memory module with distributed buffer circuits that self-calibrate read timing based on a prior write operation—represents a combination of known elements to solve a predictable problem. A strong case for obviousness can be made by combining the teachings of U.S. Patent Application Publication No. 2008/0126703 (Lee) and U.S. Patent No. 7,613,858 (Jeddeloh '858).
Summary of the Prior Art
• Lee (US 2008/0126703): This reference teaches a memory module architecture designed to improve signal integrity by using a buffer on the module's printed circuit board (PCB). The buffer is situated between the memory controller and the memory devices (DRAMs), effectively isolating the DRAMs from the main data bus. This reduces the electrical load on the memory controller, allowing for…

4. Litigation History of the Patent

Public records reflect that the 9824035 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

• Samsung Electronics Co., Ltd. et al. v. Netlist, Inc. — IPR2026-00017 · United States Patent and Trademark Office, Patent Trial and Appeal Board · filed 2025-10-27 · Not Instituted

• Micron Technology, Inc. v. Netlist, Inc. — 1:24-cv-00001 · U.S. District Court for the District of Idaho · Remanded / Closed

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]