SAMPLE — NOT LEGAL ADVICE. This response letter was generated automatically from publicly available analysis. It has NOT been reviewed by a licensed attorney and SHOULD NOT BE SENT to any party without substantial review and customization by qualified patent counsel. Use as a starting point only.

[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 8549339 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 8549339 (the "8549339 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

An analysis of United States Patent 8,549,339 reveals a technology focused on managing power and communication in multi-core processors, which has been the subject of significant litigation.
Summary of U.S. Patent 8,549,339
• Title: Processor core communication in multi-core processor
• Assignee: The current assignee is Redstone Logics LLC. The original assignee was Empire Technology Development LLC.
• Inventors: Andrew Wolfe, Marc Elliot Levitt
• Filing Date: February 26, 2010
• Issue Date: October 1, 2013
• Abstract: The patent describes techniques for handling communication between processor cores in a multi-core processor. The processor includes a first set of cores in one region that…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 8549339 Patent:

To the Senior US Patent Analyst,
The following is an analysis of the prior art cited in US Patent 8,549,339, titled "Processor core

communication in multi-core processor." This analysis is based on the patent's own cited references and an understanding of 35 U.S.C. § 102 regarding novelty and anticipation.
Analysis of Prior Art for US Patent 8,549,339
Subject Patent:
• Patent Number: 8,549,339
• Title: Processor core communication in multi-core processor
• Filing Date: February 26, 2010
• Issue Date: October 1, 2013
• Assignee: Empire Technology Development LLC.
Summary of the Invention:
US Patent 8,549,339 describes a multi-core processor architecture where different sets of processor cores can operate with independent and dynamically adjustable supply voltages and clock signals. The invention includes an interface block to facilitate communication between these different sets of cores. A key aspect is the management of this communication during changes in clock frequency, including idling and resuming communication based on the stability of phase-locked loops (PLLs)…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

Obviousness Analysis of US Patent 8549339
I. Introduction
This analysis considers the obviousness of US Patent 8,549,339, titled "Processor core communication in multi-core processor," under 35 U.S.C. § 103. The patent, filed on February 26, 2010, describes a multi-core processor architecture where different sets of processor cores can operate with independent supply voltages and clock signals. This allows for more granular power management by tailoring the power profile of a "stripe" or region of cores to their specific computational demands. The invention also addresses the communication challenges that arise between these independently-powered and clocked regions, proposing the use of interface blocks with level shifters and synchronizers.
A person of ordinary skill in the art (POSA) at the time of the invention would have been a computer architect or electrical engineer with experience in microprocessor design, particularly in the areas of multi-core processors, power management techniques like dynamic voltage and frequency scaling (DVFS), and on-chip communication…

4. Litigation History of the Patent

Public records reflect that the 8549339 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

• Redstone Logics LLC v. NXP Semiconductors, N.V. et al. — 7:24-cv-00028 · U.S. District Court for the Western District of Texas · Settled

• Redstone Logics LLC v. MediaTek, Inc. et al. — 7:24-cv-00029 · U.S. District Court for the Western District of Texas · filed 2024-01-26 · Active

• Redstone Logics LLC v. Qualcomm Incorporated et al. — 7:24-cv-00231 · U.S. District Court

for the Western District of Texas · Active

• Redstone Logics LLC v. Apple, Inc. — 7:25-cv-00183 · U.S. District Court for the Western District of Texas · Active

• Redstone Logics LLC v. Advanced Micro Devices, Inc. — 7:2025cv00182 · U.S. District Court for the Western District of Texas · filed 2025-04-18 · Active

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]