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[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 8307116 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 8307116 (the "8307116 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

An analysis of United States Patent 8,307,116 reveals the following details:
Title: Scalable bus-based on-chip interconnection networks
Assignee: University of Texas System
Inventors: Stephen W. Keckler, Boris Grot
Filing Date: June 19, 2009
Issue Date: November 6, 2012
Abstract:
The present disclosure generally relates to systems for routing data across a multinodal network. Example systems include a multinodal array having a plurality of nodes and a plurality of physical communication channels connecting the nodes. At least one of the physical communication channels may be configured to route data from a first node to two or more other destination nodes of the plurality of nodes.…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 8307116 Patent:

Analysis of Prior Art Cited in U.S. Patent 8,307,116

A thorough review of the prior art cited during the prosecution of U.S. Patent 8,307,116, "Scalable bus-based on-chip interconnection networks," provides insight into the technological landscape at the time of the invention and helps to delineate the novel aspects of the patented technology. The following analysis details the most relevant references cited by the examiner and their potential relationship to the claims of the '116 patent.
Key Cited U.S. Patents:
• U.S. Patent No. 7,490,207 B2: "Interconnect for a Multi-Processor Integrated Circuit" Publication Date: February 10, 2009 (Filed: June 29, 2004)
Description: This patent, assigned to Intel Corporation, describes a point-to-point bus interconnect for a multi-processor system on a single integrated circuit. It details a system with multiple processor cores, cache memory, and an interconnect fabric. The interconnect is designed to facilitate communication between the various components on the chip.
Potential Anticipation of Claims: The '207 patent discloses a…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

Obviousness Analysis of U.S. Patent 8,307,116
An analysis of U.S. Patent No. 8,307,116 ("the '116 patent") in light of the prior art cited during its prosecution suggests that its claims may be vulnerable to an obviousness challenge under 35 U.S.C. § 103. A person of ordinary skill in the art (POSITA) at the time of the invention (around 2009), working in the field of on-chip network design, would have been aware of the pressing need to improve the scalability and efficiency of interconnects for the increasing number of cores in multi-processor systems-on-chip (MPSoCs). The key inventive concept of the '116 patent—a grid-like network topology guaranteeing a maximum of two hops between any two nodes—could be argued as an obvious combination of known design principles and architectural elements present in the prior art.
The primary argument for obviousness rests on combining a base architecture, such as a mesh or grid interconnect, with established principles of bus-based communication and routing strategies aimed at minimizing latency.
The Independent Claims of U.S. Patent…

4. Litigation History of the Patent

Public records reflect that the 8307116 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

• Empire Technology Development LLC v. Intel Corp — 1:26-cv-00989 · Texas Western District Court · filed 2026-04-17 · Open

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or

reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]