SAMPLE — NOT LEGAL ADVICE. This response letter was generated automatically from publicly available analysis. It has NOT been reviewed by a licensed attorney and SHOULD NOT BE SENT to any party without substantial review and customization by qualified patent counsel. Use as a starting point only.

[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

June 1, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 8234483 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 8234483 (the "8234483 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

Here's a concise summary of US Patent 8234483:
Title: Memory units with packet processor for decapsulating read write access from and encapsulating response to external devices via serial packet switched protocol interface
Assignee: Edgecomm LLC (Current Assignee as of 2025-10-10) (Original Assignee: Psimast Inc)
Inventor: Viswa Nath Sharma
Filing Date: 2010-10-25
Issue Date: 2012-07-31
Abstract: A computing and communication chip architecture is provided wherein the interfaces of processor access to the memory chips are implemented as a high-speed packet switched serial interface as part of each chip. In one embodiment, the interface is accomplished through a gigabit Ethernet…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 8234483 Patent:

To identify the most relevant prior art for US patent 8234483, I will examine the patent's own

cited references as listed on Google Patents, as these are the documents the examiner and inventor considered during prosecution. The information provided in the prompt's "Obviousness" section already lists these citations, which are key for identifying potentially anticipatory prior art under 35 U.S.C. § 102.
Here's an analysis of the patent citations and their potential relevance to anticipating the claims of US8234483:
Cited Prior Art and Potential Anticipation
The patent US8234483 itself lists several prior art references in its "Cited By (Examiner)" and "Patent Citations" sections. For clarity, I will focus on the most relevant references directly discussed in the "Obviousness" section of the provided context, which are explicitly presented as foundational for the invention's background.
1. US5613071A: Method and apparatus for providing remote memory access in a distributed memory multiprocessor system
• Full Citation: US5613071A
• Publication/Filing Date: Filed: 1995-07-14 /…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

Obviousness Analysis (35 U.S.C. § 103) for US8234483
This analysis identifies combinations of prior art references that would render the claims of US patent 8234483 obvious to a person having ordinary skill in the art (POSA) at the time of the invention (priority date 2007-02-02), and articulates the motivation for such combinations.
The independent claims of US8234483 (Claims 1, 6, and 11) focus on a chip architecture where a packet processor is co-located with a memory device on a semiconductor die. This packet processor decapsulates serial packetized memory access requests (address, data, control) from an external device and encapsulates responses back to the external device, all via a high-speed packet switched serial interface.
Claim 1: Apparatus Obviousness
Combination 1: US20040019704A1 (Sano) in view of general knowledge of packet processing and serial interfaces.
• US20040019704A1 (Sano): This reference discloses a "multiple processor integrated circuit having configurable packet-based interfaces". Sano teaches using packet-based communication within an integrated…

4. Litigation History of the Patent

Public records reflect that the 8234483 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

• Untitled case — 2:25-cv-00537 · Texas Eastern District Court · Critical

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying

each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]