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[Your Name]

[Your Title]

[Your Company]

[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]

[Firm Name]

[Address]

Re: U.S. Patent No. 7547584 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 7547584 (the "7547584 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

Patent Summary: US 7,547,584 B2

Date of Analysis: May 13, 2026

Title: Method of reducing charging damage to integrated circuits during semiconductor manufacturing

Assignee: The patent was originally assigned to United Microelectronics Corp. and is currently assigned to Marlin Semiconductor Ltd.

Inventors: Ko-Ting Chen, Wen-Bin Lu, Chao-Hu Liang

Filing Date: November 16, 2006

Issue Date: June 16, 2009

Abstract: An integrated circuit die includes thereon a first device region, a second device region and a non-active region. A first implant mask, which covers the second device region and the non-active region, while exposing the first device region, is formed over the semiconductor...

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 7547584 Patent:

Prior Art Analysis for U.S. Patent No. 7,547,584

This analysis details the prior art cited in the prosecution history of U.S. Patent No. 7,547,584. Each cited reference is examined for its potential to anticipate the claims of the '584 patent under 35 U.S.C. § 102.

Based on the patent's file wrapper, the following documents were cited as prior art during the examination process:

1. U.S. Patent No. 5,998,282 (Lukaszek)

- Full Citation: US Patent 5,998,282, "Method of reducing charging damage to integrated circuits in ion implant and plasma-based integrated circuit process equipment"

- Publication Date: December 7, 1999

- Filing Date: October 21, 1997

- Description: Lukaszek discloses a method to mitigate charging damage during ion implantation and plasma processing by modifying the scribe lanes between integrated circuit dies. It teaches creating conductive paths or "shunt paths" within these scribe lanes to dissipate accumulated electrical charge to the substrate, thereby protecting the active circuit areas on the die. The patent explicitly mentions that creating such shunt...

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

Obviousness Analysis of U.S. Patent No. 7,547,584

An analysis of U.S. Patent No. 7,547,584 ("the '584 patent") in light of prior art reveals a strong case for obviousness under 35 U.S.C. § 103. The claims of the '584 patent are likely invalid as they represent an obvious combination of known techniques to solve a well-documented problem in the field of semiconductor manufacturing.

Summary of the Invention

The '584 patent, titled "Method of reducing charging damage to integrated circuits during semiconductor manufacturing," addresses the issue of electrical charge accumulation on a semiconductor wafer during processes like plasma etching and ion implantation. This charge buildup can damage sensitive components, particularly the thin gate oxides of transistors. The core of the invention is to create additional "dummy" or non-functional patterns on the integrated circuit die. These dummy patterns, which are etched or implanted at the same time as the active device features, increase the exposed surface area of the wafer. This provides additional pathways for electrical charge to...

4. Litigation History of the Patent

Public records reflect that the 7547584 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

- Unified Patents, LLC v. Marlin Semiconductor Ltd. — IPR2025-01444 · United States Patent and Trademark Office, Patent Trial and Appeal Board (PTAB) · Pending - Instituted

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying

each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]

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