

SAMPLE — NOT LEGAL ADVICE. This response letter was generated automatically from publicly available analysis. It has NOT been reviewed by a licensed attorney and SHOULD NOT BE SENT to any party without substantial review and customization by qualified patent counsel. Use as a starting point only.

[Your Name]

[Your Title]

[Your Company]

[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]

[Firm Name]

[Address]

Re: U.S. Patent No. 6963505 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 6963505 (the "6963505 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

A concise summary of US Patent 6,963,505 is as follows:

Title: Method circuit and system for determining a reference voltage

Assignee: The original assignee was Aifun Semiconductors Ltd. The current assignee of record is Spansion Israel Ltd.

Inventors: Guy Cohen

Filing Date: October 29, 2003

Issue Date: November 8, 2005

Abstract:

The present invention is a method, circuit and system for determining a reference voltage. Some embodiments of the present invention relate to a system, method and circuit for establishing a set of operating reference cells to be used in operating (e.g. reading) cells in an NVM block or array. As part of the present invention, at least a subset of cells of...

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 6963505 Patent:

Prior Art Analysis for U.S. Patent 6,963,505

Date of Analysis: April 26, 2026

Subject Patent: U.S. Patent 6,963,505, "Method, circuit and system for determining a reference voltage," filed October 29, 2003, and issued November 8, 2005.

Analyst: Senior U.S. Patent Analyst

This report details the most relevant prior art cited against U.S. Patent 6,963,505. The analysis focuses on the novelty of the patent's claims in light of pre-existing technologies, as mandated by 35 U.S.C. § 102. Each cited reference has been reviewed to determine its potential for anticipation of the claims of the '505 patent.

Key Findings:

The core invention of U.S. Patent 6,963,505 revolves around a method for selecting an optimal reference voltage for reading non-volatile memory (NVM) cells. This is achieved by reading a subset of memory cells with various possible reference levels, determining the read error rate for each level, and selecting the reference level that results in a relatively low error rate. This selected reference is then used for reading the broader memory array.

Several prior art...

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

An analysis of U.S. Patent 6,963,505 under 35 U.S.C. § 103 for obviousness reveals potential vulnerabilities based on a combination of prior art references that were available at the time of the invention. A person having ordinary skill in the art of non-volatile memory (NVM) design and operation would have been motivated to combine existing technologies to arrive at the claimed invention, rendering its claims obvious.

The core of the invention in U.S. Patent 6,963,505 lies in a method for selecting an optimal reference voltage for reading NVM cells by testing a plurality of reference levels, determining a read error rate for each, and selecting the level with a relatively low error rate. This addresses the problem of threshold voltage drift in NVM cells, which can lead to read errors.

An obviousness rejection of the claims of the '505 patent can be constructed by combining the teachings of prior art that address an iterative approach to finding optimal read parameters with a well-established understanding of error detection methods in memory systems.

For instance, the...

4. Litigation History of the Patent

Public records reflect that the 6963505 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

- SanDisk Corporation v. IPValue Management, Inc. et al. — 5:25-cv-02389 · U.S. District Court for the Northern District of California · filed 2025-03-07 · Settled
- IPValue Management, Inc. v. Western Digital Corporation — 8:25-cv-00119 · U.S. District Court for the Central District of California · filed 2025-01-22 · Ongoing

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]

DISCLAIMER. This document is a machine-generated sample. The factual assertions, prior-art citations, and legal arguments above are AI-produced and may contain errors, omissions, or outdated information. Do not transmit this letter, in whole or in part, to any party. This is not legal advice; no attorney-client relationship is created by its existence. Consult a licensed patent attorney before responding to any patent-infringement assertion.

Generated May 14, 2026 by ihatepatentrolls.com — sample only.