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[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

May 14, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 12308087 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 12308087 (the "12308087 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

Summary of U.S. Patent 12,308,087
A concise summary of U.S. Patent 12,308,087 is provided below, including details on the patent's title, assignee, inventor, key dates, and a plain-language explanation of its independent claims.
Title: Memory package having stacked array dies and reduced driver load.
Assignee: Netlist Inc.
Inventor: Hyun Lee.
Filing Date: March 14, 2022.
Issue Date: May 20, 2025.
Abstract: The patent describes a DRAM (Dynamic Random-Access Memory) package with stacked array dies. It features distinct data interconnects for different dies within the stack. Specifically, a first set of data interconnects connects to a first array die, and a separate, second set of data…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 12308087 Patent:

Based on the file history of U.S. Patent 12,308,087, the following patents were cited as prior art during prosecution. An analysis of the most relevant references is provided below.
Prior Art Analysis for US 12,308,087
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1. U.S. Patent 7,633,165 B2
• Full Citation: U.S. Patent 7,633,165 B2, "Semiconductor device and method of fabricating the same," assigned to Samsung Electronics Co., Ltd.
• Dates: Filed: October 26, 2007; Published: December 15, 2009.
• Brief Description: This patent describes a method for creating stacked semiconductor packages using Through-Silicon Vias (TSVs). It focuses on the physical structure of forming conductive paths that pass through multiple stacked chips. The invention details how to create these vertical interconnects to connect different layers of chips in a 3D package, enabling communication between them.
• Potential Anticipation of Claims: This reference is relevant background for the physical structure of stacked dies with TSVs, as mentioned in the specification of '087 (see col. 8, lines 5-11). However, U.S. Patent 7,633,165 B2 does not…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

An analysis of the obviousness of U.S. Patent 12,308,087 under 35 U.S.C. § 103 is provided below. This analysis considers whether a person having ordinary skill in the art (POSITA) would have found the claimed invention obvious at the time of the invention, based on a combination of prior art references.
Defining a Person Having Ordinary Skill in the Art (POSITA)
For the technology disclosed in US Patent 12,308,087, a POSITA would be an individual with a Bachelor's degree in Electrical Engineering, Computer Engineering, or a related field, and several years of experience in high-speed digital circuit design, memory system architecture, or semiconductor packaging. This experience would include knowledge of signal integrity principles, driver/receiver design, and the challenges associated with stacked-die (3D) integrated circuits, including the use of through-silicon vias (TSVs).
Analysis of Independent Claims
The core innovation recited in the independent claims is the use of different sized drivers for distinct data interconnects that lead to different dies within a stacked…

4. Litigation History of the Patent

Public records reflect that the 12308087 Patent has been the subject of the following litigation, which informs our view of the asserted claims and your client's enforcement posture:

• Netlist, Inc. v. Samsung Electronics Co., Ltd. et al. — 2:25-cv-00557 · U.S. District Court for the Eastern District of Texas · filed 2025-05-19 · Stayed

• Samsung Electronics Co., Ltd. et al. v. Netlist, Inc. — 1:25-cv-00626 · U.S. District Court for the District of Delaware · filed 2025-05-20 · Active

5. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]