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[Your Name]
[Your Title]
[Your Company]
[Street Address, City, State ZIP]

June 1, 2026

[Opposing Counsel Name]
[Firm Name]
[Address]

Re: U.S. Patent No. 10115439 — Response to Assertion of Infringement

Dear Counsel,

We acknowledge receipt of your correspondence asserting infringement of U.S. Patent No. 10115439 (the "10115439 Patent"). After preliminary review, we have substantial concerns about the validity, enforceability, and scope of the asserted claims, summarized below. We reserve all rights and defenses.

1. Subject Patent — Summary

US patent 10115439, titled "On-die termination of address and command signals," was issued on October 30, 2018, from an application filed on July 31, 2017. The inventors are Ian Shaeffer and Kyung Suk Oh. The original assignee was Rambus Inc., and it was later assigned to Signal LLP on October 15, 2025.
The abstract describes a system with multiple memory devices in a fly-by topology, each having on-die termination (ODT) circuitry for connection to an address and control (RQ) bus. Each memory device's ODT circuitry includes control registers for managing ODT of RQ bus signal lines. A first memory device stores a first ODT value in its control registers for termination, while a second…

2. Validity Concerns under 35 U.S.C. § 102 — Prior Art

We have identified prior-art references that, in our preliminary view, anticipate one or more asserted claims of the 10115439 Patent:

Here is an analysis of the most relevant prior art for US Patent 10115439, identified from the examiner-cited patent references within the provided patent text.
Most Relevant Prior Art for US Patent 10115439
The most relevant prior art identified are those patent citations explicitly marked as "Cited by

examiner" within the US10115439 patent document.
1. US20060107186A1
• Full Citation: US20060107186A1, International Business Machines Corporation, "System, method and storage medium for providing a high speed test interface to a memory subsystem".
• Publication/Filing Date:
Publication Date: 2006-05-18
Priority Date: 2004-10-29
• Brief Description: This patent describes a system and method primarily focused on providing a high-speed test interface for memory subsystems. It discloses memory devices with on-die termination (ODT) circuitry and a memory controller or test device that can provide a "termination control value" to set the termination. The disclosure refers to "dynamically adjustable on-die termination" and "programmable termination" within a memory system for testing…

3. Obviousness under 35 U.S.C. § 103

Independent of § 102, we believe the asserted claims are obvious in view of combinations of prior art that a person having ordinary skill in the art would have been motivated to combine:

To analyze the obviousness of US patent 10115439 under 35 U.S.C. § 103, we will examine combinations of prior art references that disclose the features claimed in US10115439. The patent generally claims a memory controller configured to program register values in a memory device to control on-die termination (ODT) impedances for address, command, chip select, and clock signals, particularly in a fly-by topology.
Key Features of US10115439's Claims:
The independent claims (Claims 1, 12, and 20) of US10115439 focus on a memory controller that:
• Drives command/address (CA) signals, chip select (CS) signals, and clock signals.
• Stores/programs register values in the memory device to control ODT impedances for these signals.
• The register values can selectively enable ODT for CS and clock signals.
• The register values can specify impedance values for the ODT.
Relevant Prior Art References and Their Disclosures:
Based on the provided patent text's "Citations" and "Family Cites Families" sections, the following references are highly relevant:
1. US7142461B2 (Micron Technology,…

4. Request

In light of the foregoing, we request that your client (i) provide a detailed claim chart identifying each accused product or service and mapping every limitation of each asserted claim, (ii) identify any prior art known to your client, including any references cited during prosecution or reexamination, and (iii) substantiate the basis for any damages or licensing demand. We are prepared to discuss the matter further once we have received and reviewed the foregoing.

Sincerely,

[Your Name]

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